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Filing Date	January 29, 1999
First Named Inventor	Andrew MacCormack
Art Unit	2623
Examiner Name	Scott E. Beliveau
Attorney Docket No.	858063.435

ENCLOSURES (*check all that apply*)

- [ ] Fee Transmittal Form
  - [ ] Fee Attached
- [ ] Amendment/Response
  - [ ] After Final
  - [ ] Affidavits/declaration(s)
- [ ] Extension of Time Request
- [ ] Express Abandonment Request
- [ ] Information Disclosure Statement and Transmittal
- [ ] Cited References
- [ ] Certified Copy of Priority Document(s)
- [ ] Response to Missing Parts under 37 CFR 1.52 or 1.53
- [ ] Response to Missing Parts/Incomplete Application
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Firm Name	Seed Intellectual Property Law Group PLLC	Customer Number	00500
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Printed Name	Timothy L. Boller		
Date	June 4, 2007	Reg. No.	47,435

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants	:	Andrew MacCormack et al.
Application No.	:	09/239,907
Filed	:	January 29, 1999
For	:	DIGITAL RECEIVER DEMULTIPLEXER
Examiner	:	Scott E. Beliveau
Art Unit	:	2623
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Date	:	June 4, 2007

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SUPPLEMENTAL APPELLANTS' BRIEF

Commissioner for Patents:

This brief is in furtherance of the Notice of Appeal, filed in this case on June 8, 2006. This brief is also in response to a Notification of Non-Compliant Appeal Brief issued by the Examiner and mailed on February 15, 2007, and to a Notification of Non-Compliant Appeal Brief mailed on May 2, 2007. The February Notification requested that: Appendix B be amended to read "None"; Section V be amended to provide reference characters for the means-plus-function elements of claims 45 and 46; and a typographical error in a heading be corrected. Applicants thank the Examiner for providing detailed comments in the Notice of Non-Complaint Appeal Brief, and have modified this brief in accordance with the Examiner's comments. Applicants note that a copy of the Final Office Action has been removed from Appendix B to comply with the Examiner's Notification of Non-Compliant Appeal Brief. The May Notification requested that the Status of Claims section of the brief be corrected. Applicants have corrected the Status of Claims section of the brief and Appendix A to identify the correct status of all of the claims, including the canceled claims.

I. REAL PARTY IN INTEREST

The real party in interest is STMicroelectronics Limited, which is the assignee of the present invention. The assignment of record is to STMicroelectronics Limited, having an address at 1000 Aztec West, Almondsbury, Bristol, BS32 4SQ United Kingdom.

II. RELATED APPEALS AND INTERFERENCES

Appellants, Appellants' legal representative, and the real party in interest are unaware of any appeal or interference which may be related to, directly affect, be directly affected by, or have a bearing on the Board's decision in the present appeal.

III. STATUS OF CLAIMS

Claims 1, 3-11, and 13-46 are currently pending in this application. All pending active claims are attached as Appendix A.

Claims 1, 3-11, 13-42, 45, and 46 stand rejected. Claims 1 and 3-10 stand rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement. Claims 39-41, 45 and 46 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 5,959,659 issued to Dokic ("Dokic"). Claims 11 and 13-20 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Dokic in view of the ADSP-2100 Family User's Manual – Chapter 4: Data Transfer (the "Manual"). Claims 21-38 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Dokic in view of U.S. Patent No. 5,844,595 issued to Blatter et al ("Blatter"). Claim 42 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Dokic in view of U.S. Patent No. 5,602,920 issued to Bestler et al ("Bestler"). Id. Claims 43 and 44 have been indicated as having allowable subject matter, but these claims stand objected to as depending from a rejected base claim. Claims 2 and 12 have been canceled.

The rejections of claims 1, 3-11, 13-41, 45 and 46 are being appealed.

IV. STATUS OF AMENDMENTS

An Amendment under 37 C.F.R. § 1.116, filed after the Final Rejection, has not been entered by Examiner Beliveau (hereinafter "Examiner"). In the Amendment, Applicants sought to clarify the language of claims 1 and 3-10 to address the Examiner's concerns and to amend the drawings to address other concerns raised by the Examiner. The Amendment also

contained new claims directed to the subject matter of allowable claims 43 and 44. Applicants subsequently offered to cancel the new claims, so that the issues in dispute could be clearly presented to the Board for review, but the Examiner indicated the Amendment would not be entered, even if the new claims were canceled. In the event of a remand, Applicants are prepared to resubmit the proposed amendments.

V. SUMMARY OF CLAIMED SUBJECT MATTER

This Application claims priority to Great Britain Application No. GB9802093, filed January 30, 1998. The following summary discusses the subject matter of the appealed claims along with references to portions of the specification and drawings that provide support for the claims. The references are provided for exemplary purposes and are not intended to restrict the scope of the claims to the particular embodiments corresponding to the references provided.

The present invention generally relates to demultiplexing of a digital data stream in a receiver, so as to retain only those parts of the digital data stream required by the receiver. The invention relates particularly but not exclusively to such a receiver circuit in a television system having a digital set-top-box receiver.

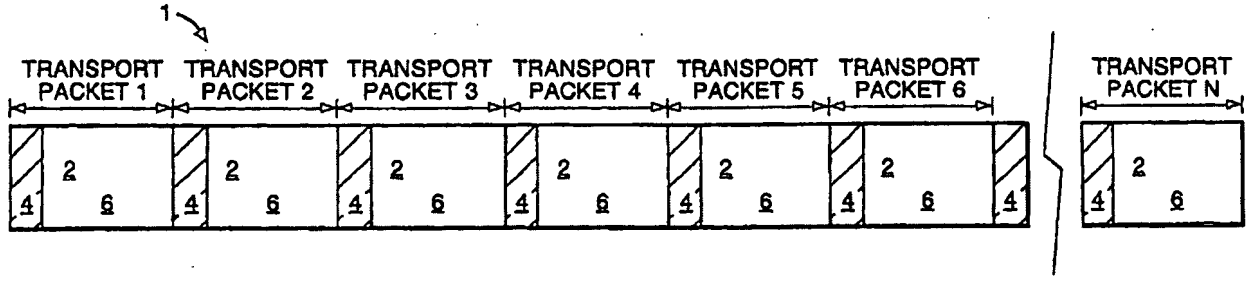


FIG. 1

Figure 1 of the present application, reproduced above for the Board's convenience, illustrates a portion of a transport stream 1 which is composed of a series of N transport packets 2. Each transport packet 2 comprises a transport packet header 4 and a transport packet payload 6. The transport stream is a bit stream which carries in the transport packet payloads 6 information for recreating, for example, a number of different television programs. The transport stream is formed by source encoding the television programs. The

transport stream is then typically channel encoded for transmission (by satellite or cable) and channel decoded on its reception to reproduce the transport stream. The transport stream is then source decoded to recreate a selected one of the different television programs. A particular television program is recreated using three types of information (audio information, video information and tables of program information). Each transport packet 2 is preferably associated with a particular television program, a particular source encoding time and a particular one of the information types. The individual transport packets are time division multiplexed to form the transport stream and allow the real-time recreation of any one of the different television programs from the transport stream. To recreate a television program the transport stream is sequentially demultiplexed to recover only the transport payloads 6 of audio information, video information and tables of program information which are associated with the selected television program. The recovered payloads are then decoded and used to recreate the television program.

An embodiment of the present invention provides a programmable transport interface in which the demultiplexing of an incoming data stream is programmable so as to enable different standards to be multiplexed without placing a burden on the main processor of the decoder.

An example embodiment of a programmable transport interface is illustrated in Figure 2, which is reproduced for the Board's convenience.

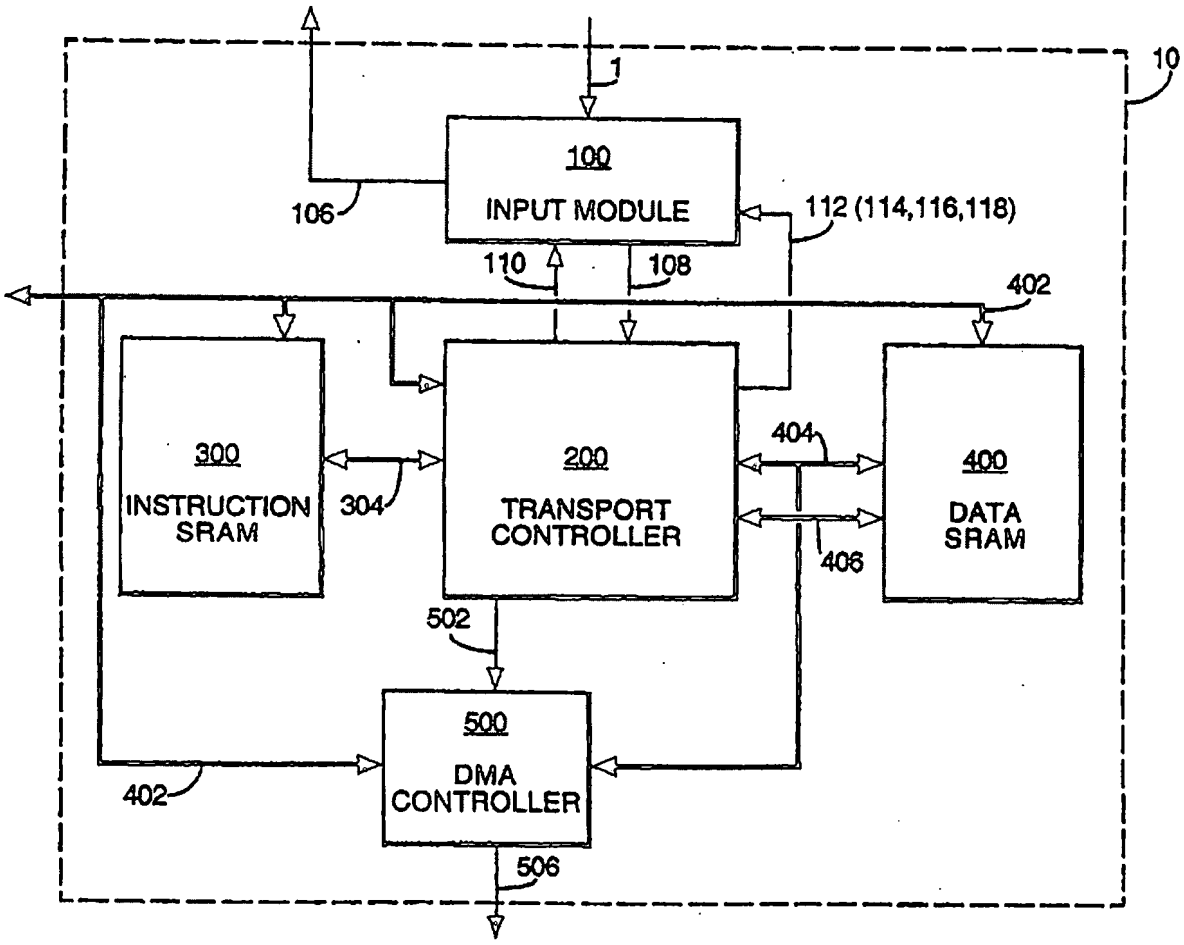


FIG. 2

For example, the embodiment of the receiver of **claim 1** demultiplexes a digital data stream, the digital data stream including data packets each having a packet identifier, so as to retain only those data packets required by the receiver. The receiver comprises:

- an input module for receiving and processing the digital data stream;
- a memory for storing packet identifiers corresponding to data packets required by the receiver and separate from the input module;
- a first control circuit for controlling the storage in the memory of the packet identifiers;
- a second control circuit for extracting a packet identifier from a data packet in the digital data stream; and

- a third control circuit for receiving the extracted packet identifier and determining whether such matches one of the packet identifiers stored in the memory, for setting a match signal to the second control circuit responsive to a match, and for outputting an address in the memory responsive to a match, wherein the second control circuit accesses the address in the memory to retrieve control information associated with the packet identifier and controls processing of the input data packet responsive to the match signal by the input module.

Support for independent claim 1 can be found not only in Figure 2 but also in claim 1 as originally filed, on page 5, line 23, to page 6, line 5, Specification as Filed, and on page 4, line 28, to page 5, line 9, Substitute Specification. Additional support for claim 1 in the form of an example embodiment of a transport controller of the programmable transport interface is provided in Figure 3, reproduced below for the Board's convenience. Further support can be found in the description of Figure 3 provided on page 13, line 22, to page 16, line 18, Specification as Filed, and on page 11, line 27, to page 14, line 10, Substitute Specification.

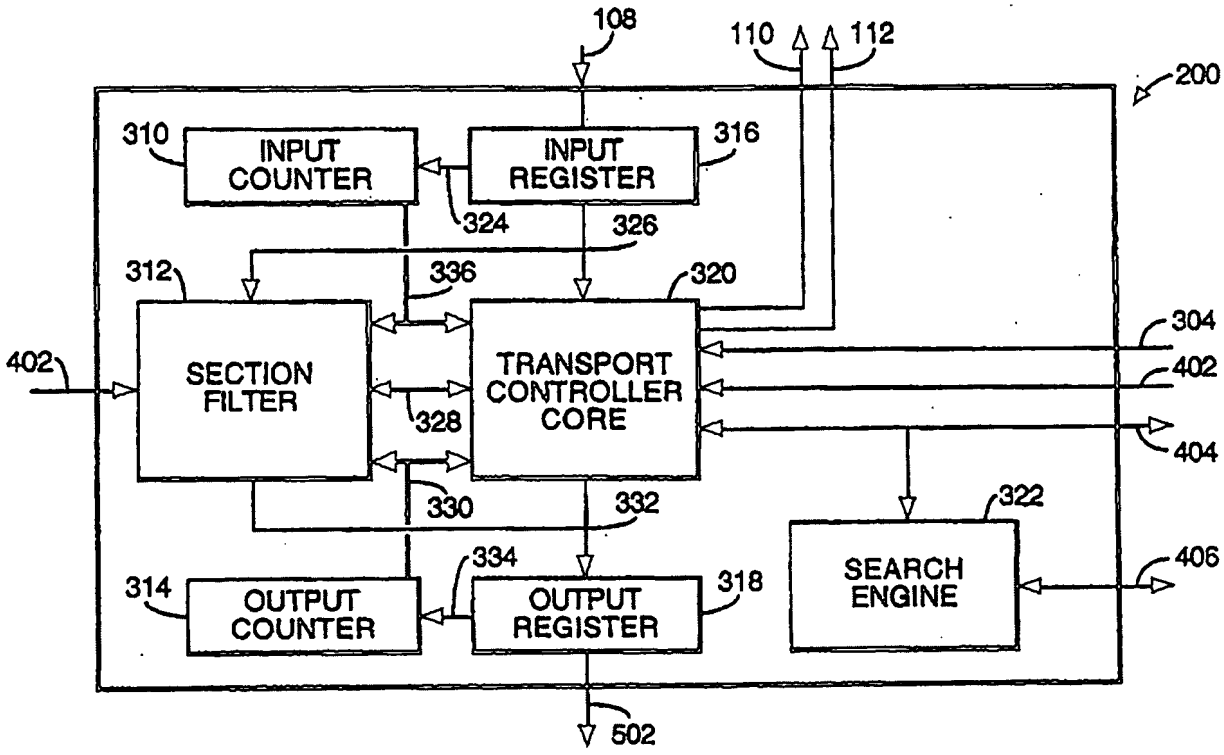


FIG. 3

In addition, support in the form of an example embodiment of the search engine of the transport controller of Figure 3 is provided in Figure 4, also reproduced below for the Board's convenience. Further support can be found in the description of Figure 4 provided on page 16, line 20 to page 23, line 22, Specification as Filed, and on page 14, line 11, to page 20, line 14, Substitute Specification.

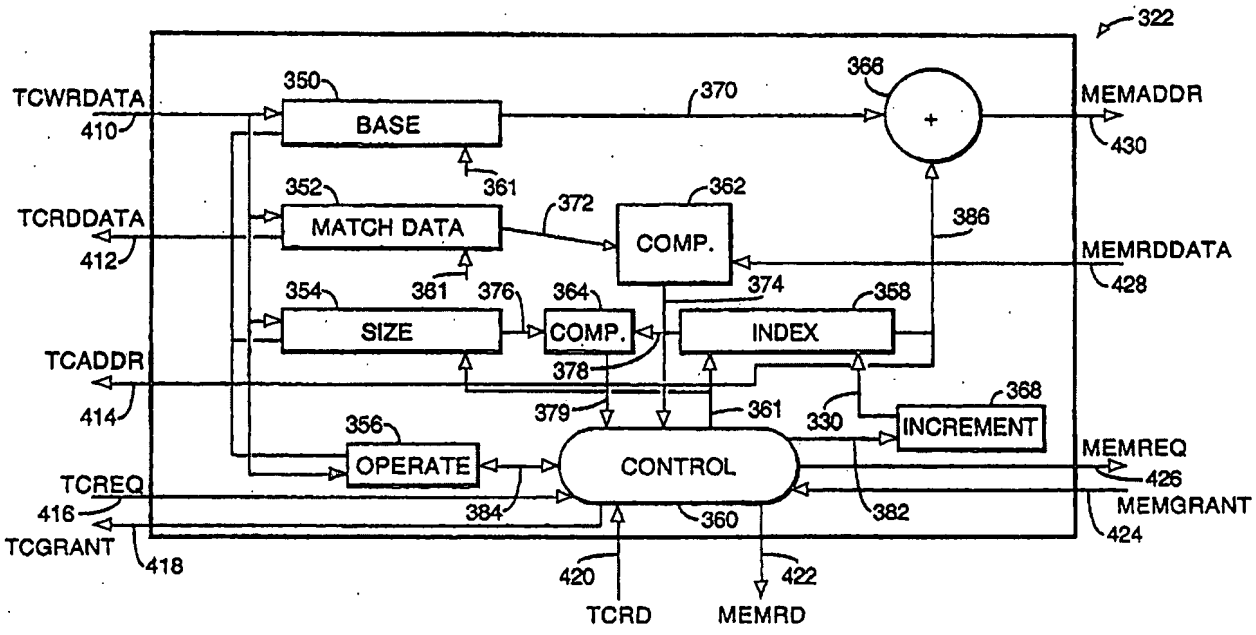


FIG. 4

An embodiment of the set top box of **claim 10** includes a receiver for demultiplexing a digital data stream, the digital data stream including data packets each having a packet identifier, so as to retain only those data packets required by the receiver, the receiver comprising the same elements as the receiver in claim 1. Support for the receiver as claimed in independent claim 10 can be found in the portions of the application listed above in reference to claim 1. Support for a set top box including a receiver can be found on page 1, lines 9-12, page 7, lines 10-13, Specification as Filed, and on page 1, lines 6-7, page 6, lines 10-12, Substitute Specification. Applicants submit that independent claims 1 and 10 do not contain any means-plus-function limitations.

An embodiment of a method of **claim 11** for demultiplexing a digital data stream input to a receiver, the digital data stream including data packets each having a packet identifier, so as to retain only those data packets required by the receiver, comprises the steps of:

- inputting the digital data stream;
- storing in a memory separate from the data stream and under the control of a first control circuit, packet identifiers of data packets required by the receiver;
- extracting, under the control of a second control circuit, a packet identifier from a data packet in the input digital data stream;
- determining, under the control of a third control circuit, whether the extracted packet identifier matches one of the stored packet identifiers;
- setting a match signal responsive to a match determined by the third control circuit;
- outputting, responsive to a match and under the control of the third control circuit, an address in the memory;
- accessing, under the control of the second control circuit, the address in memory;
- retrieving control information associated with the packet identifier and stored at such address; and
- demultiplexing, under the control of the second control circuit, the input data packet responsive to the match signal.

Support for independent claim 11 can be found in claim 11 as originally filed, on page 6, lines 3-17, Specification as Filed, and on page 5, lines 10-20, Substitute Specification. In another example, an embodiment of a method of **claim 20** for decoding a broadcast digital data signal in a set top box comprises steps substantially similar to those of claim 11. Support for the steps of independent claim 20 can be found in the portions of the application listed above in reference to claim 11. Support for decoding a broadcast digital data signal in a set top box can be found in claim 20 as originally filed, on page 1, lines 9-12, page 7, lines 10-13, Specification as Filed, and on page 1, lines 6-7, page 6, lines 10-12, Substitute Specification.

Applicants note that the Examiner objected to the Figures for failing to illustrate the steps recited in independent claims 11 and 20, and Applicants offered in their Response after Final to add a figure illustrating the recited steps (which were disclosed in the specification as filed). As noted above, the Amendment After Final was not entered. Applicants are prepared to amend the figures to address the Examiner's objection in the event of a remand. Applicants submit that independent claims 11 and 20 do not contain any step-plus-function limitations.

An embodiment of the receiver of **claim 21** includes a receiver for demultiplexing a digital data stream, the digital data stream including data packets each having a packet identifier, so as to retain only those data packets required by the receiver, the receiver comprising:

- input circuitry for receiving the digital data stream;
- a first data structure for storing addressing information that is accessed based on packet identifiers;
- a second data structure for storing control information that is accessed based on addressing information extracted from the first data structure;
- a first control circuit for extracting a packet identifier from a data packet in the digital data stream input to the input circuitry; and
- a second control circuit for receiving the extracted packet identifier and determining whether such matches one of the packet identifiers in the first data structure, for setting a match signal to the first control circuit responsive to a match, and outputting addressing information responsive to a match, wherein the first control circuit accesses the second data structure to retrieve control information associated with the addressing information and demultiplexes the input data packet responsive to the match signal.

Support for independent claim 21 can be found in Figures 2 and 3. In addition, support in the form of an example embodiment of the advantageous interconnection of arrays, associated with transport packets, in the memory of the programmable transport interface of Figure 2 is provided in Figure 5, also reproduced below for the Board's convenience.

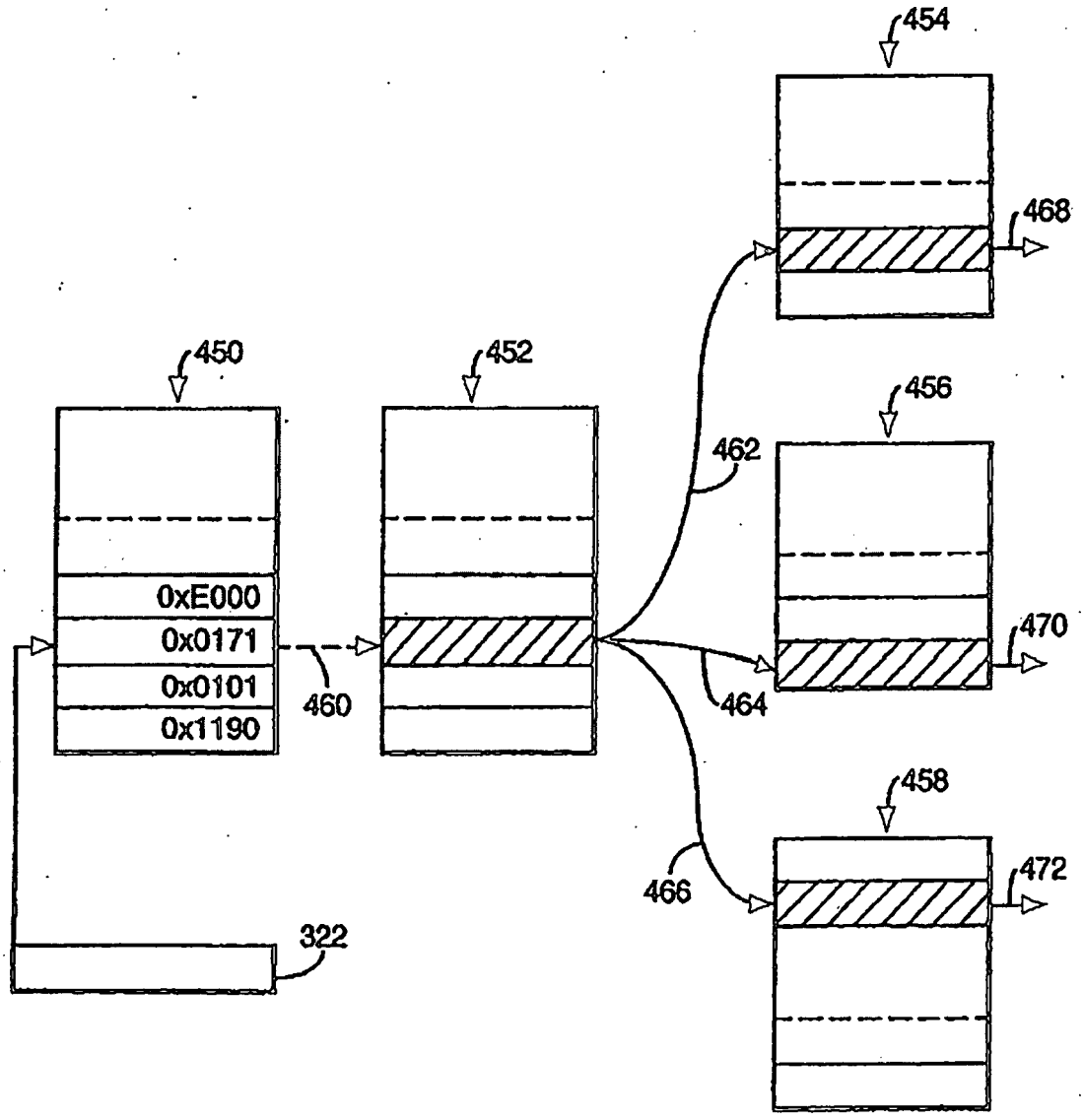


FIG. 5

Further support for claim 21 can be found in the description of Figure 5 provided on page 23, line 24 to page 24, line 11, Specification as Filed, and on page 20, line 15, to page 21, line 3, Substitute Specification. An embodiment of the set top box of **claim 29** includes a receiver for demultiplexing a digital data stream, the digital data stream including data packets each having a packet identifier, so as to retain only those data packets required by the receiver,

the receiver comprising the same elements as the receiver of claim 21. Support for the receiver as claimed in independent claim 29 can be found in the portions of the application listed above in reference to claim 21. Support for a set top box including a receiver can be found on page 1, lines 9-12, page 7, lines 10-13, Specification as Filed, and on page 1, lines 6-7, page 6, lines 10-12, Substitute Specification.

More detail in the form of an example embodiment of a digital broadcast system incorporating a programmable transport interface is provided in Figure 6, also reproduced below for the Board's convenience. Further support can be found in the description of Figure 6 provided on page 24, line 13 to page 27, line 5, Specification as Filed, and on page 21, line 4, to page 23, line 15, Substitute Specification.

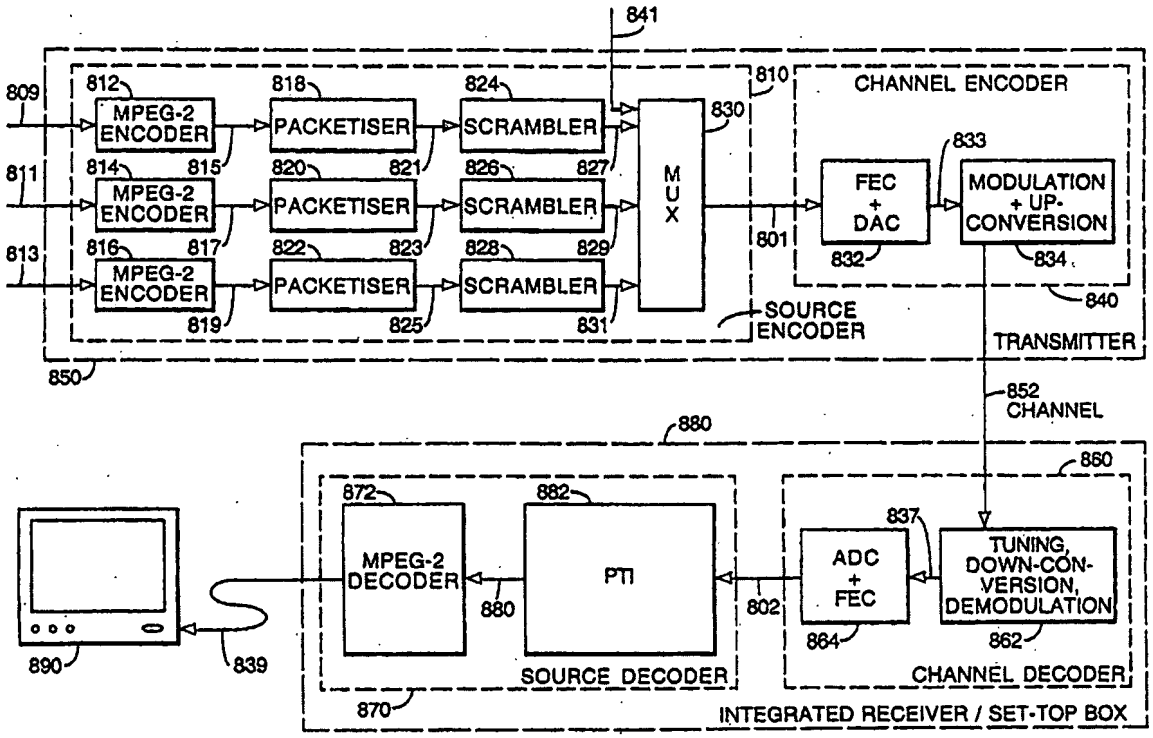


FIG. 6

Applicants submit that independent claims 21 and 29 do not contain any means-plus-function limitations.

An embodiment of a method of demultiplexing a digital data stream of **claim 30,** the digital data stream including data packets each having a packet identifier, so as to retain only those data packets required by the receiver, comprises the steps of:

inputting the digital data stream;

storing control information in a first data structure;

storing packet identifiers and corresponding addressing information in a second data structure;

extracting, under the control of a first control circuit, a packet identifier from a data packet in the input digital data stream;

determining, under the control of a second control circuit, whether the extracted packet identifier matches one of the packet identifiers in the second data structure;

setting a match signal responsive to a match determined by the second control circuit;

outputting addressing information from the second data structure responsive to a match;

retrieving, under control of the first control circuit and based on the outputted addressing information, control information from the first data structure; and

demultiplexing, under the control of the first control circuit, the input data packet responsive to the match signal.

Support for independent claim 30 can be found can be found in Figure 5, the description of Figure 5 provided on page 23, line 24 to page 24, line 11, Specification as Filed, and on page 20, line 15, to page 21, line 3, Substitute Specification. An embodiment of the method of decoding a broadcast digital data signal in a set top box of **claim 38** includes the same steps as the method of claim 30. Support for the method as claimed in independent claim 38 can be found in the portions of the application listed above in reference to claim 30. Support for a set top box including a receiver can be found on page 1, lines 9-12, page 7, lines 10-13, Specification as Filed, and on page 1, lines 6-7, page 6, lines 10-12, Substitute Specification.

More detail in the form of an example embodiment of a digital broadcast system incorporating a programmable transport interface is provided in Figure 6, also reproduced above for the Board's convenience. Further support can be found in the description of Figure 6

provided on page 24, line 13 to page 27, line 5, Specification as Filed, and on page 21, line 4, to page 23, line 15, Substitute Specification.

Applicants submit that independent claims 30 and 38 do not contain any step-plus-function limitations.

In another example, an embodiment of the receiver of **claim 39** for processing a packetized digital data stream includes:

- an input module to receive and process a data packet;
- a memory;
- a receiver processor to control storage of desired packet identifiers and associated control information in the memory; and
- a transport controller having a transport processor to extract a packet identifier from a packet in the input module and a search engine to search the memory for a match of the extracted packet identifier to a desired packet identifier stored in the memory, wherein responsive to a match the transport processor retrieves from the memory control information associated with the desired packet identifier stored in the memory and controls processing of the received data packet by the input module based on the retrieved control information.

Support for independent claim 39 can be found not only in Figure 2 but also in the description of Figure 2 found on page 8, line 17, to page 13, line 20, Specification as Filed (filed on January 29, 1999), and on page 7, line 12, to page 11, line 26, Substitute Specification (filed on November 14, 2002).

The embodiment of claim 42 additionally includes the transport processor generating a control signal to control processing of a packet by the input module based on associated control information retrieved from the memory and "wherein the input module descrambles a packet in response to the control signal." Support for the embodiment of claim 42 can be found in Figure 2 and the description of Figure 2 found on page 8, line 17, to page 13, line 20, Specification as Filed, and on page 7, line 12, to page 11, line 26, Substitute Specification.

As another example, the embodiment of claim 43 additionally includes the transport processor generating a control signal to control processing of a packet by the input

module based on associated control information retrieved from the memory and "wherein the input module passes a data payload to the transport controller in response to the control signal." Support for the embodiment of claim 43 can be found in Figure 2 and the description of Figure 2 found on page 8, line 17, to page 13, line 20, Specification as Filed, and on page 7, line 12, to page 11, line 26, Substitute Specification.

The embodiment of claim 44 additionally includes the transport processor generating a control signal to control processing of a packet by the input module based on associated control information retrieved from the memory, the input module passing a data payload to the transport controller in response to the control signal, and "wherein the transport controller reformats the data payload based on the control information and passes the reformatted data payload to the input module for output in an alternative output stream." Support for the embodiment of claim 44 can be found in Figure 2 and the description of Figure 2 found on page 8, line 17, to page 13, line 20, Specification as Filed, and on page 7, line 12, to page 11, line 26, Substitute Specification.

Independent **Claim 45** and **Claim 46** include means plus function elements. According to 37 C.F.R. § 41.37(c)(1)(v), such means plus function elements "must be identified and the structure, material, or acts described in the specification as corresponding to each claimed function must be set forth with reference to the specification by page and line number, and to the drawing, if any, by reference characters." Accordingly, the following shows claims 45 and 46 together with the required information in parentheses.

45. A receiver for processing a packetized digital data stream, the receiver comprising:

means for receiving a data packet in the digital data stream **(page 8, lines 17-22; page 8, line 35, to page 9, line 12; page 9, lines 22-26; page 26, lines 31-32; Specification as Filed) (page 7, lines 12-16; page 7, line 24, to page 8, line 6; page 8, lines 12-15; page 23, lines 7-8; Substitute Specification) (Figure 2, input module 100)**

means for retrieving control information associated with a received data packet **(page 11, lines 18-35; page 15, lines 24-33; page 16, lines 10-18; page 18, lines 11-17; page 21, lines 19-24; page 23, lines 4-13; page 26, lines 34-36; Specification as Filed) (page 10, lines 3-15; page 13, lines 19-25; page 14, lines 5-10; page 15, line 27, to page 16, line 2; page**

18, lines 21-25; page 20, lines 3-9; page 23, lines 9-11; Substitute Specification) (Figure 2, data SRAM 400, transport controller 200, interconnections 402, 404, 406; Figure 3, transport controller core 320, search engine 322, interconnections 402, 404, 406); and

means for controlling processing of a received data packet by the means for receiving a data packet **(page 9, line 28, to page 10, line 13; page 10, lines 25-28; page 11, lines 35-37; page 12, lines 9-11; page 22, lines 8-13; page 26, lines 31-32; page 26, lines 34-36; Specification as Filed) (page 8, line 16, to page 9, line 3; page 9, lines 11-13; page 10, lines 15-16; page 10, lines 22-24; page 19, lines 10-13; page 23, lines 7-8; page 23, lines 9-13; Substitute Specification) (Figure 2, transport controller 200, interconnect 110, control signals 112 (114, 116, 118); Figure 3, transport controller core 320, interconnect 110, control signal 112).**

46. The receiver of claim 45 wherein the means for retrieving control information comprises a memory **(Figure 2, data SRAM 400)** storing packet identifiers and control information associated with desired data packets in the digital data stream, a search engine **(Figure 3, search engine 322)** and a transport processor **(part of transport controller core 320) (page 14, second paragraph; page 15, lines 24-33; page 16, lines 10-18; Specification as Filed) (page 12, lines 28-29; page 13, lines 19-25; page 14, lines 5-10; Substitute Specification).**

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

1. Whether claims 1 and 3-10 comply with the written description and enablement requirements of 35 U.S.C. § 112, first paragraph.

2. Whether claims 39-41 are anticipated under 35 U.S.C. § 102(e) by Dokic.

3. Whether claims 45 and 46 are anticipated under 35 U.S.C. § 102(e) by Dokic.

4. Whether claims 11 and 13-20 are rendered obvious under 35 U.S.C. § 103(a) by Dokic in view of the Manual.

5. Whether claims 21-38 are rendered obvious under 35 U.S.C. § 103(a) by Dokic in view of Blatter.

6. Whether claim 42 is rendered obvious under 35 U.S.C. § 103(a) by Dokic in view of Bestler.

7. Whether claims 43 and 44, which the Examiner has indicated as having allowable subject matter, depend from a properly rejected base claim.

VII. ARGUMENT

Although the Examiner has rejected each of claims 1, 3-11, 13-42, 45, and 46 under either 35 U.S.C. §§ 102, 103, or 112, Final Office Action, the Examiner has not made out a *prima facie* case on any of the grounds for rejection.

A. Claims 1 and 3-10 Are Enabled and Comply With the Written Description Requirement

To support the written description and enablement rejections, the Examiner bears the initial burden of establishing that the written description in the specification is inadequate to enable any person skilled in the art to make and use the invention. To establish a *prima facie* case of lack of enablement, the Examiner "bears the burden of setting forth a reasonable explanation as to why it believes that the scope of protection by that claim is not adequately enabled by the description of the invention provided in the specification of the application; this includes, of course, providing sufficient reasons for doubting any assertions in the specification as to the scope of enablement." *In re Wright*, 999 F.2d 1557, 1561-1562 (Fed. Cir. 1993). Regarding written description, the Examiner must establish that the disclosure of the application does not reasonably convey to a person of ordinary skill in the art that the inventor had possession of the invention when the application was filed. Vas-Cath, Inc. v. Mahurkar, 935 F.2d 1555, 1563-1564 (Fed. Cir. 1991).

In the Final Office Action, the Examiner rejected Claims 1 and 3-10 under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement and as not enabled. The Examiner's argument is based on a misinterpretation of the claims. Specifically, the Examiner contends the claim 1 and 10 recite an input module setting a match signal. Claims 1 and 10, however, do not recite an input module setting a match signal.

Claim 1 recites a receiver for demultiplexing a digital data stream, the digital data stream including data packets each having a packet identifier, so as to retain only those data packets required by the receiver, the receiver comprising an input module for receiving and processing the digital data stream; a memory for storing packet identifiers corresponding to data packets required by the receiver and separate from the input module; a first control circuit for controlling the storage in the memory of the packet identifiers; a second control circuit for extracting a packet identifier from a data packet in the digital data stream; and a ***third control circuit*** for receiving the extracted packet identifier and determining whether such matches one of the packet identifiers stored in the memory, ***for setting a match signal*** to the second control circuit responsive to a match, and for outputting an address in the memory responsive to a match, wherein the second control circuit accesses the address in the memory to retrieve control information associated with the packet identifier and controls processing of the input data packet responsive to the match signal by the input module. Appendix A, Claim 1 (emphasis added).

As also amended, claim 10 recites a set top box including a receiver for demultiplexing a digital data stream, the digital data stream including data packets each having a packet identifier, so as to retain only those data packets required by the receiver. Appendix A, Claim 10. The receiver of claim 10 comprises the same elements as the receiver in claim 1 above. *Id.*

The Examiner notes that the specification discloses that the match signal is generated by the third control circuit. Final Office Action, Page 7. Applicants agree that some embodiments described in the specification (as well as those claimed in claims 3 and 10) involve the third control circuit generating a match signal under certain circumstances. See Figures 1-3, claim 1 as originally filed, the Specification as filed on page 5, line 23, to page 6, line 5, page 13, line 22, to page 16, line 18. The Examiner then argues that both claim 1 and claim 10 specify that the input module sets the match signal, and therefore rejects both claims as failing to comply with the written description requirement. Id. However, claims 1 and 10 do not specify that the input module sets the match signal. See Claims 1 and 10 ("a ***third control circuit*** ... ***for setting a match signal*** to the second control circuit responsive to a match") (emphasis added). The Examiner's rejection is based on a misreading of both claims. The Examiner's own analysis on page 7 of the Final Office Action states "the particular match signal as disclosed in the

specification and **required by the claim to be generated by the 'third control circuit.'**[*sic*]" (emphasis added). Thus, there is no confusion about whether the input module or the third control circuit sets the match signal, and the claims do not recite the input module generating the match signal.

Claims 3-9 depend from claim 1. Appendix A. For the foregoing reasons, the Examiner has not established a prima facie case of non-enablement or lack of written description, and thus, the Section 112 rejections of claims 1 and 3-10 should be withdrawn.

B. Claims 39-41 Are Not Anticipated by Dokic

Under 35 U.S.C. § 102, "[a] claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 U.S.P.Q.2d 1051, 1053 (Fed. Cir. 1987). "The identical invention must be shown in as complete detail as is contained in the ... claim." Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 U.S.P.Q.2d 1913, 1920 (Fed. Cir. 1989). Here, the Examiner has failed to establish a *prima facie* case of anticipation for claims 39-41, 45, or 46. The Examiner erred in asserting that Dokic teaches or enables each of the claimed elements, either expressly or inherently, as interpreted by one of ordinary skill in the art.

Independent claim 39 recites: "A receiver for processing a packetized digital data stream, the receiver comprising: an input module to receive and process a data packet; a memory; a receiver processor to control storage of desired packet identifiers and associated control information in the memory; and a transport controller having a transport processor to extract a packet identifier from a packet in the input module and a search engine to search the memory for a match of the extracted packet identifier to a desired packet identifier stored in the memory, wherein responsive to a match the transport processor retrieves from the memory control information associated with the desired packet identifier stored in the memory and controls processing of the received data packet by the input module based on the retrieved control information." Claims 40 and 41 depend from claim 39.

The Examiner points to demultiplexer section 104 as the claimed input module, memory 205 as the claimed memory, host processor 106 as the claimed receiver processor, and

digital signal processor 102 as the claimed transport processor, and to the description thereof at column 7, l. 49, through col. 9, l. 6, and col 13, ln. 13-26.

There is no indication in the cited portion of Dokic that the host processor 106 controls storage of desired packet identifiers ***and*** associated control information in the memory 205. The cited portion of Dokic refers to loading a PID filtering table from the host processor 106 into the memory 205. Dokic then defines the PID filtering table as containing the desired PIDs. There is no suggestion that the PID filtering table contain associated control information, or that such information be stored anywhere else in the memory 205. *See* Dokic, column 8, ln. 26-53. In addition, there is no indication in the cited portion of Dokic that the digital signal processor 102, responsive to a match, retrieves from the memory 205 control information associated with the desired packet identifier. Accordingly, Dokic does not anticipate claims 39-41.

To the extent the Examiner suggests that the type of packet is the "associated control information," Dokic does not teach, suggest or motivate storing the type of packet in the memory 205 (or retrieving the type of packet from the memory 205). Instead, Dokic teaches that the location in the PID filtering table where the PID is stored corresponds to the type of data packet. To the extent the Examiner points to the discussion of selecting a default program in Dokic (see col. 8, ln. 53-67), the default program data in Dokic is recovered from the transport stream when a PID filtering table is not available from the host processor 106. There is no suggestion in Dokic that the host processor 106 controls the storage of default PIDs in the memory 205 (or the storage of associated control information in the memory 205).

C. Claims 45 and 46 Are Not Anticipated by Dokic

Independent claim 45 separately recites: "means for receiving a data packet in the digital data stream; means for retrieving control information associated with a received data packet; and means for controlling processing of a received data packet by the means for receiving a data packet." As discussed above, Dokic does not teach, motivate or suggest retrieving control information associated with a received data packet. Claim 46 depends from claim 45 and further specifies that the means for retrieving control information comprises "a memory storing packet identifiers and control information associated with desired data packets in

the digital data stream, a search engine and a transport processor." Accordingly, Applicants respectfully submit that claims 39-41, 45 and 46 are not anticipated by Dokic.

D. The Examiner has Failed to Establish a Prima Facie *Case that Dokic in view of the Manual Renders Claims 11 and 13-20 Obvious.*

The Examiner initially bears the burden of establishing a *prima facie* case of obviousness. In re Bell, 26 U.S.P.Q.2d 1529 (Fed. Cir. 1993); In re Oetiker, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); In re Piasecki, 745 F.2d 1468, 1472, 223 U.S.P.Q. 785, 788 (Fed. Cir. 1984); MPEP § 2142. An Applicant may attack an obviousness rejection by showing that the Examiner has failed to properly establish a *prima facie* case or by presenting evidence tending to support a conclusion of non-obviousness. In re Fritch, 972 F.2d at 1265.

In order for an examiner to establish a *prima facie* case that an invention, as defined by a claim at issue, is obvious the examiner must: (1) show some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine the reference teachings; (2) there must be a reasonable expectation of success; and (3) the prior art reference (or the combined references) must teach or suggest all the claim limitations. MPEP § 2142. "The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure." MPEP § 2143. The level of skill in the art cannot be relied upon to provide the suggestion to combine the references. MPEP § 2143.01 (citing Al-Site Corp. v. VSI Int'l Inc., 174 F.3d 1308, 50 U.S.P.Q.2d 1161 (Fed. Cir. 1999)). The mere fact that the references ***can*** be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. MPEP § 2143.01 (citing In re Mills, 916 F.2d 680, 16 U.S.P.Q. 2d 1430 (Fed. Cir. 1990)).

Moreover, a reference must be viewed as a whole, including portions that would lead away from the claimed invention. MPEP § 2141.03 (citing W.L. Gore & Assoc., Inc. v. Garlock, Inc., 721 F.2d 1540, 220 U.S.P.Q. 303 (Fed. Cir. 1983)). If the proposed modification would change the principles of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims *prima facie* obvious. MPEP § 2143.01 (citing In re Ratti, 270 F.2d 810, 123 U.S.P.Q. 349 (CCPA 1959)).

Here, the Examiner has failed to establish a *prima facie* case of obviousness for claims 11, 13-20. The Examiner has rejected Claims 11 and 13-20 under 35 USC 103(a) as rendered obvious over Dokic in view of the ADSP-2100 Family User's Manual – Chapter 4: Data Transfer. Applicants respectfully traverse the Examiner's rejection.

Independent claims 11 and 20 recite, "inputting the digital data stream; storing in a memory separate from the data stream and under the control of a first control circuit, packet identifiers of data packets required by the receiver; extracting, under the control of a second control circuit, a packet identifier from a data packet in the input digital data stream; determining, under the control of a third control circuit, whether the extracted packet identifier matches one of the stored packet identifiers; setting a match signal responsive to a match determined by the third control circuit; outputting, responsive to a match and under the control of the third control circuit, an address in the memory; accessing, under the control of the second control circuit, the address in memory; retrieving control information associated with the packet identifier and stored at such address; and demultiplexing, under the control of the second control circuit, the input data packet responsive to the match signal," (or similar language).

Dokic is not an appropriate primary reference because the Examiner is using an unreasonable interpretation of the claimed memory to include the memory 205 **and** data buffers 200 and 202 of Dokic. Buffers 200 and 202 are not separate from the data stream and do not store "packet identifiers corresponding to data packets required by the receiver" for determining "whether the extracted packet identifier matches one of the stored packet identifiers." Buffers 200 and 202 are circular buffers controlled by framing logic to load **all** data packets in the transport stream, whether the packets are required or not. See Column 7, line 66 to Column 8, line 19. Thus, buffers 200 and 202 are not separate from the data stream. Thus, Dokic is not an appropriate primary reference for claims 11 and 13-20.

The Examiner first argues that the buffers 200 and 202 meet the claim limitations for the memory if they store desired packet identifiers even for an instant. The Examiner ignores the limitation that the memory storing the packet identifiers be "separate from the data stream." The Examiner next argues that the specification discloses buffers in the data stream and storage of data packets from the data stream in the memory. The Examiner fails to provide specific citations to the specification and does not tie this argument to corresponding limitations in the

claims. In any event, the specification as originally filed separately illustrates and describes the data stream. *See, e.g.* Original Specification, Figures 1 and 2 and the description thereof on pages 7-12. An embodiment of the data stream is illustrated and described as comprising the transport stream 1, the input module 100, interconnect 108, interconnect 110, the alternative output stream 106, the transport controller 200, the interconnect 502, the direct memory access controller 500 and the data output stream 506. See Figures 2 and 3. The specification as originally filed also separately illustrates and describes the data SRAM 400. *See, e.g.*, Figure 2 and the description of the data SRAM 400 on pages 11-13. There is no suggestion that the data stream or the transport stream includes the data SRAM 400, passes through the data SRAM 400, or is buffered in the data SRAM 400, and Applicants respectfully submit one of skill in the art would not interpret the specification in this manner. Applicants further note that the claims do not address whether the transport stream comprises input buffers, or prohibit the memory from also storing data packets (or portions thereof).

Further, the Examiner admits that Dokic does not disclose or suggest "outputting an address", but claims this is suggested by the Manual, which describes the operation of a circular buffer. The problem with this argument is that the circular buffer of Dokic that the Examiner suggests combining with the Manual is the circular buffer 200/202, which the Examiner admits stores the "entire packet" and which as discussed above cannot be the claimed memory as recited. Accordingly, Applicants respectfully submit claims 11 and 13-20 are not rendered obvious by Dokic taken in combination with the Manual. Furthermore, if Dokic were modified such that the circular buffers stored either packet identifiers required by the receiver or addressing information, Dokic would not function as intended, as the stored information would be replaced (and thus lost) if the buffers were operated in a circular fashion and there would be no place to store the digital data stream as it was received if the buffers were not operated in a circular fashion or were used to store other information. Further, to the extent the address is an address of one of the buffers, it is still an address of a buffer in the data stream, and thus would not be an address in a memory separate from the data stream, as recited. Accordingly, Applicants respectfully submit that claims 11 and 13-20 are not rendered obvious by the combination of Dokic and the Manual.

E. The Examiner has Failed to Establish a Prima Facie *Case that Dokic in View of Blatter Renders Claims 21-38 Obvious.*

Claims 21-38 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Dokic in view of Blatter. Applicants respectfully traverse the Examiner's contention that claims 21-38 are obvious over Dokic in view of Blatter and further submit that the Examiner has failed to establish a *prima facie* case of obviousness. The Examiner's burden of proof is set forth above.

Claims 21 and 29 recite "a first data structure for storing addressing information that is accessed based on packet identifiers ... a second data structure for storing control information that is accessed based on addressing information extracted from the first data structure ... outputting addressing information responsive to a match ... wherein the first control circuit accesses the second data structure to retrieve control information associated with the addressing information." Similarly, claim 30 recites ""storing control information in a first data structure; storing packet identifiers and corresponding addressing information in a second data structure ... outputting addressing information from the second data structure responsive to a match [and] retrieving ... based on the outputted addressing information, control information from the first data structure" and claim 38 similarly recites "storing, in a first data structure, control information; storing, in a second data structure, packet identifiers ... and addressing information corresponding to the packet identifiers ... outputting, responsive to a match, addressing information stored in the second data structure [and] retrieving ... based on the outputted addressing information, control information from the first data structure."

The Examiner admits that Dokic does not disclose or suggest the claimed first **and** second data structures. The Examiner contends memory 205 of Dokic is a first data structure, without explaining how or whether it satisfies the claim limitations. The Examiner also points to units 45 of Blatter as both the first data structure and the second data structure. The Examiner does not identify how to combine unit 45 with Dokic so as to achieve the claimed invention. Further, one of skill in the art would not be motivated to combine Dokic with Blatter. Dokic is directed to "a decoder having a decoupled hardware architecture for demultiplexing and decoding a digital data stream." Dokic, Column 1, lines 6-9. Dokic specifically decouples demultiplexing from decoding the digital data stream and expressly limits the "interpretation

capabilities" of the digital signal processor 102 in order to speed up the demultiplexing so data can promptly be displayed. Dokic, Column 4, lines 48-60. The only data Dokic indicates is stored in the memory 205 is the PID look-up table, which Dokic teaches preferable contains only the required PIDs. There is no teaching or suggestion in Dokic that the PID look-up table contain addressing information that is accessed based on packet identifiers or control information that is accessed based on addressing information. Modifying the digital signal processor 102 of Dokic to contain two data structures with the second data structure containing control information to be retrieved and either employed by the digital signal processor to interpret the data stream or provided to an external circuit by the digital signal processor would defeat the purpose of limiting the capabilities of the digital signal processor in order to speed up the demultiplexing, and would change the principles of operation of Dokic. *See* MPEP § 2143.01(VI) ("The proposed modification cannot change the principle of operation of a reference."); *In re Ratti*, 270 F.2d 810, 813, 123 U.S.P.Q. 349, 352 (C.C.P.A. 1959). Claims 22-28 depend from claim 21 and claims 31-37 depend from claim 30. Accordingly, Applicants submit that claims 21-38 are not rendered obvious by Dokic in view of Blatter, and the Examiner has failed to establish a *prima facie* case of obviousness.

F. The Examiner has Failed to Establish a Prima Facie *Case that Dokic in View of Bestler Renders Claim 42 Obvious.*

Claim 42 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Dokic in view of Bestler. Applicants respectfully traverse the Examiner's contention that claim 42 is obvious over Dokic in view of Bestler. The Examiner's burden of establishing a *prima facie* case is set forth above.

Claim 42 depends from claim 39. The Examiner does not contend that the features of claim 39 that are missing from Dokic, as discussed above, are taught, suggested or motivated by Bestler.

Accordingly, Applicants respectfully submit that claim 42 is not rendered obvious by Dokic in view of Bestler and that the Examiner has not established a *prima facie* case of obviousness.

G. *The Allowable Subject Matter of Claims 43-44 Do Not Depend From a Validly Rejected Base Claim.*

Claims 43 and 44 have been indicated as having allowable subject matter, but these claims stand objected to as depending from a rejected base claim. As noted above, Applicants respectfully traverse the Examiner's contention that claim 39, from which claims 43 and 44 ultimately depend, is a validly rejected base claim. Accordingly, Applicants traverse the objections to claims 43 and 44 as well.

VIII. CLAIMS APPENDIX

A copy of the claims involved in the appeal are attached hereto as Appendix A.

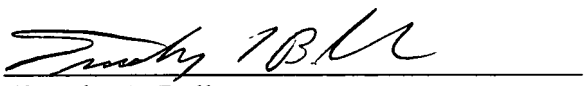
IX. EVIDENCE APPENDIX

None. Applicants note a copy of the Final Office Action was removed from this Appendix to comply with the Examiner's Notice of Non-Compliant Appeal Brief.

X. RELATED PROCEEDINGS APPENDIX

The Related Proceedings Appendix is attached as Appendix C. Applicants note that there are no related proceedings of which Applicants are aware.

Respectfully submitted,
Seed Intellectual Property Law Group PLLC



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Enclosures:
Appendix A – Claims Involved in the Appeal
Appendix B – Evidence Appendix
Appendix C – Related Proceedings Appendix

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APPENDIX A

Claims Involved in the Appeal

1. (Previously Presented) A receiver for demultiplexing a digital data stream, the digital data stream including data packets each having a packet identifier, so as to retain only those data packets required by the receiver, the receiver comprising:

an input module for receiving and processing the digital data stream;

a memory for storing packet identifiers corresponding to data packets required by the receiver and separate from the input module;

a first control circuit for controlling the storage in the memory of the packet identifiers;

a second control circuit for extracting a packet identifier from a data packet in the digital data stream; and

a third control circuit for receiving the extracted packet identifier and determining whether such matches one of the packet identifiers stored in the memory, for setting a match signal to the second control circuit responsive to a match, and for outputting an address in the memory responsive to a match, wherein the second control circuit accesses the address in the memory to retrieve control information associated with the packet identifier and controls processing of the input data packet responsive to the match signal by the input module.

2. (Canceled)

3. (Previously Presented) The receiver of claim 1 wherein responsive to the control information the second control circuit controls the transfer of the input data packet to a destination address identified by the control information.

4. (Previously Presented) The receiver of claim 1, wherein responsive to the control information the second control circuit retrieves a data payload from the input module, processes the data payload and transfers the processed data payload to a destination address identified by the control information.

5. (Previously Presented) The receiver of claim 1 wherein responsive to the match signal not being set, the second control circuit instructs the input module to discard the input data packet.

6. (Original) The receiver of claim 1 in which the digital data stream is an MPEG 2 encoded stream.

7. (Previously Presented) The receiver of claim 3 in which the input data packet comprises a packetized elementary stream.

8. (Previously Presented) The receiver of claim 4 in which the data payload comprises program specific information, and the receiver further comprises a filter controlled by the second control circuit for filtering sections in the data payload so as to retain only those data packets having sections required by the receiver.

9. (Original) The receiver of claim 1 in which first control circuit is a receiver processor, the second control circuit is a transport processor, and the third control circuit is a search engine.

10. (Previously Presented) A set top box including a receiver for demultiplexing a digital data stream, the digital data stream including data packets each having a packet identifier, so as to retain only those data packets required by the receiver, the receiver comprising:

an input module for receiving the digital data stream;

a memory for storing packet identifiers corresponding to data packets required by the receiver and separate from the input module;

a first control circuit for controlling the storage in the memory of the packet identifiers;

a second control circuit for extracting a packet identifier from a data packet in the digital data stream; and

a third control circuit for receiving the extracted packet identifier and determining whether such matches one of the packet identifiers stored in the memory, for setting a match signal to the second control circuit responsive to a match, and for outputting an address in the memory responsive to a match, wherein the second control circuit accesses the address in the memory to retrieve control information associated with the packet identifier and controls processing of the input data packet responsive to the match signal by the input module.

11. (Previously Presented) A method of demultiplexing a digital data stream input to a receiver, the digital data stream including data packets each having a packet identifier, so as to retain only those data packets required by the receiver, comprising the steps of:

inputting the digital data stream;

storing in a memory separate from the data stream and under the control of a first control circuit, packet identifiers of data packets required by the receiver;

extracting, under the control of a second control circuit, a packet identifier from a data packet in the input digital data stream;

determining, under the control of a third control circuit, whether the extracted packet identifier matches one of the stored packet identifiers;

setting a match signal responsive to a match determined by the third control circuit;

outputting, responsive to a match and under the control of the third control circuit, an address in the memory;

accessing, under the control of the second control circuit, the address in memory;

retrieving control information associated with the packet identifier and stored at such address; and

demultiplexing, under the control of the second control circuit, the input data packet responsive to the match signal.

12. (Canceled)

13. (Previously Presented) The method of claim 11 further comprising the step of:

transferring, under the control of the second control circuit, the input data packet to a destination address identified by the control information.

14. (Previously Presented) The method of claim 11 further comprising the steps of:

processing, under the control of the second control circuit, the input data packet in dependence on the control information; and

transferring, under the control of the second control circuit, the processed input data packet to a destination address identified by the control information.

15. (Original) The method of claim 11 in which the step of demultiplexing comprises discarding the input data packet responsive to the match signal not being set.

16. (Original) The method of claim 11 in which the digital data stream is an MPEG 2 encoded stream.

17. (Previously Presented) The method of claim 16 in which the input data packet comprises a packetized elementary stream.

18. (Previously Presented) The method of claim 16 in which the input data packet comprises program specific information, and wherein said demultiplexing step comprises:

filtering sections in the input data packet so as to retain only those data packets having sections required by the receiver.

19. (Original) The method of claim 11 in which the step of determining a match comprises systematically searching the memory.

20. (Previously Presented) A method of decoding a broadcast digital data signal in a set top box comprising:

inputting the digital data stream;

storing in a memory separate from the data stream and under the control of a first control circuit, packet identifiers of data packets required by the set-top-box;

extracting, under the control of a second control circuit, a packet identifier from a data packet in the input digital data stream;

determining, under the control of a third control circuit, whether the extracted packet identifier matches one of the stored packet identifiers;

setting a match signal responsive to a match determined by the third control circuit;

outputting, responsive to a match and under the control of the third control circuit, an address in the memory;

accessing, under the control of the second control circuit, the address in memory;

retrieving control information associated with the packet identifier and stored at such address; and

demultiplexing, under the control of the second control circuit, the input data packet responsive to the match signal.

21. (Previously Presented) A receiver for demultiplexing a digital data stream, the digital data stream including data packets each having a packet identifier, so as to retain only those data packets required by the receiver, the receiver comprising:

input circuitry for receiving the digital data stream;

a first data structure for storing addressing information that is accessed based on packet identifiers;

a second data structure for storing control information that is accessed based on addressing information extracted from the first data structure;

a first control circuit for extracting a packet identifier from a data packet in the digital data stream input to the input circuitry; and

a second control circuit for receiving the extracted packet identifier and determining whether such matches one of the packet identifiers in the first data structure, for setting a match signal to the first control circuit responsive to a match, and outputting addressing information responsive to a match, wherein the first control circuit accesses the second data structure to retrieve control information associated with the addressing information and demultiplexes the input data packet responsive to the match signal.

22. (Previously Presented) The receiver of claim 21 wherein responsive to the control information the first control circuit controls the transfer of the input data packet to a destination address identified by the control information.

23. (Previously Presented) The receiver of claim 21, wherein responsive to the control information the first control circuit processes the input data packet and transfers the processed input data packet to a destination address identified by the control information.

24. (Previously Presented) The receiver of claim 21 wherein responsive to the match signal not being set, the first control circuit discards the input data packet.

25. (Previously Presented) The receiver of claim 21 in which the digital data stream is an MPEG 2 encoded stream.

26. (Previously Presented) The receiver of claim 22 in which the input data packet comprises a packetized elementary stream.

27. (Previously Presented) The receiver of claim 23 in which the input data packet comprises program specific information, and the receiver further comprises a filter

controlled by the first control circuit for filtering sections in the input data packet so as to retain only those data packets having sections required by the receiver.

28. (Previously Presented) The receiver of claim 21 in which first control circuit is a transport processor, and the second control circuit is a search engine.

29. (Previously Presented) A set top box including a receiver for demultiplexing a digital data stream, the digital data stream including data packets each having a packet identifier, so as to retain only those data packets required by the receiver, the receiver comprising:

input circuitry for receiving the digital data stream;

a first data structure for storing addressing information that is accessed based on packet identifiers;

a second data structure for storing control information that is accessed based on addressing information extracted from the first data structure;

a first control circuit for extracting a packet identifier from a data packet in the digital data stream input to the input circuitry; and

a second control circuit for receiving the extracted packet identifier and determining whether such matches one of the packet identifiers in the first data structure, for setting a match signal to the first control circuit responsive to a match, and outputting addressing information responsive to a match, wherein the first control circuit accesses the second data structure to retrieve control information associated with the addressing information and demultiplexes the input data packet responsive to the match signal.

30. (Previously Presented) A method of demultiplexing a digital data stream input to a receiver, the digital data stream including data packets each having a packet identifier, so as to retain only those data packets required by the receiver, comprising the steps of:

inputting the digital data stream;

storing control information in a first data structure;

storing packet identifiers and corresponding addressing information in a second data structure;

extracting, under the control of a first control circuit, a packet identifier from a data packet in the input digital data stream;

determining, under the control of a second control circuit, whether the extracted packet identifier matches one of the packet identifiers in the second data structure;

setting a match signal responsive to a match determined by the second control circuit;

outputting addressing information from the second data structure responsive to a match;

retrieving, under control of the first control circuit and based on the outputted addressing information, control information from the first data structure; and

demultiplexing, under the control of the first control circuit, the input data packet responsive to the match signal.

31. (Previously Presented) The method of claim 30 further comprising the step of:

transferring, under the control of the first control circuit, the input data packet to a destination address identified by the retrieved control information.

32. (Previously Presented) The method of claim 30 further comprising the steps of:

processing, under the control of the first control circuit, the input data packet based on the control information; and

transferring, under the control of the first control circuit, the processed input data packet to a destination address identified by the retrieved control information.

33. (Previously Presented) The method of claim 30 in which the step of demultiplexing comprises discarding the input data packet responsive to the match signal not being set.

34. (Previously Presented) The method of claim 30 in which the digital data stream is an MPEG 2 encoded stream.

35. (Previously Presented) The method of claim 34 in which the input data packet comprises a packetized elementary stream.

36. (Previously Presented) The method of claim 34 in which the input data packet comprises program specific information, and wherein said demultiplexing step comprises:

filtering sections in the input data packet so as to retain only those data packets having sections required by the receiver.

37. (Previously Presented) The method of claim 30 in which the step of determining a match comprises systematically searching the second data structure.

38. (Previously Presented) A method of decoding a broadcast digital data signal in a set top box comprising:

inputting the digital data stream;

storing, in a first data structure, control information;

storing, in a second data structure, packet identifiers required by the set-top-box and addressing information corresponding to the packet identifiers;

extracting, under the control of a first control circuit, a packet identifier from a data packet in the input digital data stream;

determining, under the control of a second control circuit, whether the extracted packet identifier matches one of the packet identifiers stored in the second data structure;

setting a match signal responsive to a match determined by the second control circuit;

outputting, responsive to a match, addressing information stored in the second data structure;

retrieving, under control of the first control circuit and based on the outputted addressing information, control information from the first data structure; and

demultiplexing, under the control of the first control circuit, the input data packet responsive to the match signal.

39. (Previously Presented) A receiver for processing a packetized digital data stream, the receiver comprising:

an input module to receive and process a data packet;

a memory;

a receiver processor to control storage of desired packet identifiers and associated control information in the memory; and

a transport controller having a transport processor to extract a packet identifier from a packet in the input module and a search engine to search the memory for a match of the extracted packet identifier to a desired packet identifier stored in the memory, wherein responsive to a match the transport processor retrieves from the memory control information associated with the desired packet identifier stored in the memory and controls processing of the received data packet by the input module based on the retrieved control information.

40. (Previously Presented) The receiver of claim 39 wherein the transport processor generates a control signal to control processing of a packet by the input module based on associated control information retrieved from the memory.

41. (Previously Presented) The receiver of claim 40 wherein the input module discards a packet in response to the control signal.

42. (Previously Presented) The receiver of claim 40 wherein the input module descrambles a packet in response to the control signal.

43. (Previously Presented) The receiver of claim 40 wherein the input module passes a data payload to the transport controller in response to the control signal.

44. (Previously Presented) The receiver of claim 43 wherein the transport controller reformats the data payload based on the control information and passes the reformatted data payload to the input module for output in an alternative output stream.

45. (Previously Presented) A receiver for processing a packetized digital data stream, the receiver comprising:

means for receiving a data packet in the digital data stream;

means for retrieving control information associated with a received data packet; and

means for controlling processing of a received data packet by the means for receiving a data packet.

46. (Previously Presented) The receiver of claim 45 wherein the means for retrieving control information comprises a memory storing packet identifiers and control information associated with desired data packets in the digital data stream, a search engine and a transport processor.

APPENDIX B
Evidence Appendix

None.

APPENDIX C

Related Proceedings Appendix

There are no known related proceedings.